

# Secure Embedded SLC NAND SSD PBGA

## FEATURES

- Storage Capacities:
  - 4GBYTE and 8GBYTE\*\*
- Environment conditions:
  - Operating temperature: -40°C to 85°C
  - Storage temperature: -55°C to 125°C
- SLC Flash
  - 3.3V single power supply
  - 256 Bytes of attribute memory
- Power consumption
  - 3.3V ± 10%
  - Active mode: Read, Write, Erase operation: 95 mA (Typ), 150 (Max)
  - Sleep mode: 10 mA (Typ); TBD mA (Max)
  - Secure erase: 85 mA (Max) (4GB)
- Interface modes
  - PC card memory mode
  - PC card I/O mode
  - True IDE mode
- Less than 1 Error in 10<sup>14</sup> bits read
- MTBF > 4,000,000 hours
- High shock & vibration tolerance
- W/E Endurance: 4,000,000 write/erase cycles
- High performance
  - Interface Transfer speed in PIO mode 6
  - Typical write: 30 MBytes/s in ATA PIO mode 6
  - Typical read: 45 MBytes/s in ATA PIO mode 6
  - On card ECC up to 4 Bytes per 512 Byte data sector
- Dimensions:
  - 27mm x 22mm x 2.60mm
- Highly resistant to data corruption due to power loss
- Single device connector free solution for embedded environments
- Sophisticated wear leveling firmware
- Enhanced reliability with a 1.27mm pitch; eutectic tin-lead solder ball
- Same form, fit and functionality as W7NxxxVHxxBI with the following exceptions: M9 = EXTPWR and L11 = EXTTRIG for secure erase

- Built in ATA/PCMCIA 2.1, and compact flash 3.0 interface capability
- Hardware & software triggered security erase that meets:\*\*\*
  - NISPOM DoD 5220.22-M
  - NSA - 130-2
  - Airforce AFSSI - 5020
  - Army AR380-19
  - Navy NAVSO P-5234-26
- Page read operation
- Page Program time: 200µs (Typ)
- Block erase time: 1.5ms (Typ)
- Program/Erase lockout during transition
- Data transfer rate: Up to 66MB/s UDMA mode 4  
Up to 25MB/s PIO mode 6 or MDMA mode 4
- Sustained read: Up to 45 MBytes/s
- Sustained write: Up to 30 MBytes/s with interleaving
- Random read: Up to 35 MBytes/s
- Random write: Up to 6 MBytes/s

## DESCRIPTION

The W7NxxxVHxxBISx series embedded SLC NAND SSD PBGA is based on flash technology. This product is constructed with 32bit RISC base controller and SLC NAND flash memory devices. They operate from a single 3.3 volt power supply. Capacity ranges from 4GB to 8GB\*\*.

\* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

\*\* 8GB capacity is TBD.

\*\*\* This feature will not be available for sample production

TABLE 1

| Item            | Size  | Performance |
|-----------------|-------|-------------|
| W7N2G16VHxxBISx | 4GB   | 3.0 to 3.60 |
| W7N4G16VHxxBISx | 8GB** |             |



FIGURE 1 – 224 PBGA PIN CONFIGURATION – TOP VIEW

|   | 1  | 2  | 3  | 4                 | 5                          | 6                            | 7                | 8                | 9              | 10                            | 11      | 12  | 13 | 14 | 15 |
|---|----|----|----|-------------------|----------------------------|------------------------------|------------------|------------------|----------------|-------------------------------|---------|-----|----|----|----|
| A |    | NC | NC | NC                | NC                         | NC                           | NC               | NC               | NC             | NC                            | NC      | NC  | NC | NC | NC |
| B | NC | NC | NC | NC                | NC                         | NC                           | NC               | NC               | NC             | NC                            | NC      | NC  | NC | NC | NC |
| C | NC | NC | NC | NC                | NC                         | NC                           | NC               | NC               | NC             | NC                            | NC      | NC  | NC | NC | NC |
| D | NC | NC | NC | GND               | GND                        | IOCS16#<br>(IOIS16#)<br>(WP) | IORDY<br>(WAIT#) | DMACK#<br>(REG#) | CSEL#          | PDIAG#<br>(STSCHG#)<br>(BVD1) | GND     | GND | NC | NC | NC |
| E | NC | NC | NC | GND               | DASP#<br>(SPKR#)<br>(BVD2) | DMARQ<br>(INPACK#)           | WE#              | CS1#<br>(CE2#)   | CS0#<br>(CE1#) | IORQ#                         | D00     | GND | NC | NC | NC |
| F | NC | NC | NC | Vcc               | NC                         | INTRQ<br>(IREQ#)<br>(READY)  | IOWR#            | ATASEL#<br>(OE#) | D08            | D14                           | D09     | D10 | NC | NC | NC |
| G | NC | NC | NC | Vcc               | Vcc                        | NC                           | GND              | GND              | GND            | GND                           | D01     | D15 | NC | NC | NC |
| H | NC | NC | NC | Vcc               | NC                         | NC                           | GND              | GND              | GND            | D07                           | D04     | Vcc | NC | NC | NC |
| J | NC | NC | NC | RESET#<br>(RESET) | NC                         | GND                          | GND              | GND              | Vcc            | D12                           | Vcc     | Vcc | NC | NC | NC |
| K | NC | NC | NC | NC                | A03                        | A02                          | A05              | A10              | D05            | D03                           | D11     | Vcc | NC | NC | NC |
| L | NC | NC | NC | GND               | A00                        | A01                          | A06              | A09              | D06            | D13                           | EXTTRIG | GND | NC | NC | NC |
| M | NC | NC | NC | GND               | GND                        | A04                          | A07              | A08              | EXTPWR         | D02                           | GND     | GND | NC | NC | NC |
| N | NC | NC | NC | NC                | NC                         | NC                           | NC               | NC               | NC             | NC                            | NC      | NC  | NC | NC | NC |
| P | NC | NC | NC | NC                | NC                         | NC                           | NC               | NC               | NC             | NC                            | NC      | NC  | NC | NC | NC |
| R | NC | NC | NC | NC                | NC                         | NC                           | NC               | NC               | NC             | NC                            | NC      | NC  | NC | NC | NC |

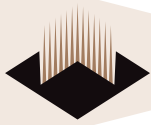
NOTE: Pin assignments are identical to the W7NxxxVHxxBI standard embedded SLC NAND SSD BGA except for M9 - EXTPWR and L11 - EXTTRIG.



## WN7xxxVHxxBISx Secure NAND SSD PBGA Features:

1. **Secure Erase:** A hardware or software triggered erase which will erase all internal customer data, including data which may have been left in blocks which have been set aside because of wear leveling or blocks which have been declared bad by the flash controller. This Secure Erase will be completed within 10 (Typ) sec of initiation.
2. **Power Loss:** Once a Secure Erase has been initiated, if power is lost, then the Secure Erase will complete the next time power is restored.
3. **EXTPWR:** An external power pin is provided to which a backup power supply can be connected. If  $V_{CC}$  is removed from the BGA, the part will continue to operate from the backup power supply. If a battery or capacitor based temporary power source is attached, a Secure Erase could be completed even after the main power on  $V_{CC}$  is lost. For the 4GB W7N2G16VH1SBISx, a maximum of 85 mA is needed for ~10 sec during Secure Erase.
4. **Security Erase:** The following Security Erase protocol standards will be supported as options. The customer may select one of these standard protocols to be included:
  - a. NISPOM DoD 5220.22-M
  - b. NSA-130-2
  - c. Air Force AFSSI-5020
  - d. Army AR380-19
  - e. Navy NAVSO P-5239-26
5. The W7NxxxVHxxBISx will initiate a Secure Erase:
  - a. by a logic low level applied to the EXTTRIG pin for >50ms. The EXTTRIG pin must be high for >200ms on power-up before arming to allow a Secure Erase command from this source. The EXTTRIG pin has an internal 4.7K pull-up resistor to 3.3V, and is de-bounced, so a momentary contact to ground or an open-drain output can also be used.
  - b. by the receipt of a serial "Secure Erase" command on the EXTTRIG pin. The serial "Secure Erase" command uses Manchester like encoding on this single signal line.
  - c. Additional data available on secure app. note:

Upon initiation of a Secure Erase, the simple erase discussed in item 1 above will be completed first, then the erase protocol which has been specified by the customer will commence. This allows the data to be purged quickly for an emergency situation, and also allows the data to be erased to the specified protocol in a longer time frame.



ENVIRONMENTAL CHARACTERIZATION

Table with 2 columns: Item, Performance. Rows include Temperature Cycle, Humidity, Vibration, Shock, and Altitude.

PRODUCT RELIABILITY

Table with 2 columns: Item, Value. Rows include MTBF (@ 25°C), Data reliability, and Endurance.

PRODUCT PERFORMANCE

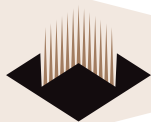
Table with 2 columns: Item, Performance (PIO mode 6 true IDE). Rows include Read Transfer Rate, Write Transfer Rate, and Controller Overhead.

ABSOLUTE MAXIMUM RATINGS

Table with 5 columns: Symbol, Parameter, Min, Max, Unit. Rows include TA, TSTG, VG, and VCC.

CURRENT CONSUMPTION FOR SECURE ERASE

Table with 5 columns: Symbol, Parameter, Temp, Max, Unit. Rows show Icc values at 85°C, 25°C, and -40°C.



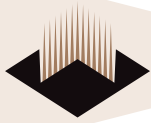
**DC ELECTRICAL CHARACTERISTICS**

| Symbol           | Parameter                                 | Min  | Max                  | Units | Notes  |
|------------------|---|------|----------------------|-------|--------|
| V <sub>CC</sub>  | Supply Voltage Range                      | 3.0  | 3.6                  | V     |        |
| V <sub>IL</sub>  | Input LOW Voltage                         | -0.3 | +0.8                 | V     | —      |
| V <sub>IH</sub>  | Input HIGH Voltage                        | 2.0  | V <sub>CC</sub> +0.3 | V     | —      |
| V <sub>OL</sub>  | Output LOW Voltage                        | —    | 0.45                 | V     | at 4mA |
| V <sub>OH</sub>  | Output HIGH Voltage                       | 2.4  |                      | V     | -1mA   |
| I <sub>CC</sub>  | Operating Current, V <sub>CC</sub> = 3.3V |      |                      |       |        |
|                  | Sleep Mode                                | —    | TBD                  | mA    | —      |
|                  | Operating                                 | —    | 165                  | mA    | —      |
| I <sub>LI</sub>  | Input Leakage Current                     | —    | ±10                  | µA    | —      |
| I <sub>LO</sub>  | Output Leakage Current                    | —    | ±10                  | µA    | —      |
| C <sub>I,O</sub> | Input/Output Capacitance                  | —    | 10                   | pF    | —      |

**ATTRIBUTE MEMORY READ AND WRITE AC CHARACTERISTICS**

3.3 V ±0.3V

| Symbol                  | Parameter                           | Min | Max | Units |
|-------------------------|-------------------------------------|-----|-----|-------|
| t <sub>cR</sub>         | Read Cycle Time                     | 250 | —   | ns    |
| t <sub>a(A)</sub>       | Address Access Time                 | —   | 250 | ns    |
| t <sub>a(CE)</sub>      | Card Enable Access Time             | —   | 250 | ns    |
| t <sub>a(OE)</sub>      | Output Enable Access Time           | —   | 125 | ns    |
| t <sub>dis(CE)</sub>    | Output Disable time from CE#        | —   | 100 | ns    |
| t <sub>dis(OE)</sub>    | Output Disable time from OE#        | —   | 100 | ns    |
| t <sub>en(CE)</sub>     | Output Enable time from CE#         | 5   | —   | ns    |
| t <sub>en(OE)</sub>     | Output Enable time from OE#         | 5   | —   | ns    |
| t <sub>v(A)</sub>       | Data valid time from address change | 0   | —   | ns    |
| t <sub>su(A)</sub>      | Address Setup Time                  | 30  | —   | ns    |
| t <sub>h(A)</sub>       | Address Hold Time                   | 20  | —   | ns    |
| t <sub>su(CE)</sub>     | Card Enable Setup Time              | 0   | —   | ns    |
| t <sub>h(CE)</sub>      | Card Enable Hold Time               | 20  | —   | ns    |
| t <sub>cW</sub>         | Write Cycle Time                    | 250 | —   | ns    |
| t <sub>w(WE)</sub>      | Write Pulse Time                    | 150 | —   | ns    |
| t <sub>su(A-WEH)</sub>  | Address setup time for WE#          | 30  | —   | ns    |
| t <sub>su(CE-WEH)</sub> | Card Enable setup time for WE#      | 30  | —   | ns    |
| t <sub>su(D-WEH)</sub>  | Data setup time for WE#             | 80  | —   | ns    |
| t <sub>h(D)</sub>       | Data hold time                      | 30  | —   | ns    |
| t <sub>dis(WE)</sub>    | Output disable time from WE#        | —   | 100 | ns    |
| t <sub>en(WE)</sub>     | Output enable time from WE#         | 5   | —   | ns    |
| t <sub>su(OE-WE)</sub>  | Output Enable setup time for WE#    | 10  | —   | ns    |
| t <sub>h(OE-WE)</sub>   | Output Enable hold time from WE#    | 10  | —   | ns    |



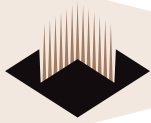
**COMMON MEMORY READ AND WRITE AC CHARACTERISTICS**

| Symbol                  | Parameter                           | Min | Max | Units |
|-------------------------|-------------------------------------|-----|-----|-------|
| t <sub>cR</sub>         | Read Cycle Time                     | 80  | —   | ns    |
| t <sub>a(A)</sub>       | Address Access Time                 | —   | 55  | ns    |
| t <sub>a(CE)</sub>      | Card Enable Access Time             | —   | 55  | ns    |
| t <sub>a(OE)</sub>      | Output Enable Access Time           | —   | 45  | ns    |
| t <sub>dis(CE)</sub>    | Output Disable time from CE#        | —   | 45  | ns    |
| t <sub>dis(OE)</sub>    | Output Disable time from OE#        | —   | 45  | ns    |
| t <sub>en(CE)</sub>     | Output Enable time from CE#         | 5   | —   | ns    |
| t <sub>en(OE)</sub>     | Output Enable time from OE#         | 5   | —   | ns    |
| t <sub>v(A)</sub>       | Data valid time from address change | 0   | —   | ns    |
| t <sub>su(A)</sub>      | Address Setup Time                  | 10  | —   | ns    |
| t <sub>h(A)</sub>       | Address Hold Time                   | 10  | —   | ns    |
| t <sub>su(CE)</sub>     | Card Enable Setup Time              | 0   | —   | ns    |
| t <sub>h(CE)</sub>      | Card Enable Hold Time               | 10  | —   | ns    |
| t <sub>cW</sub>         | Write Cycle Time                    | 80  | —   | ns    |
| t <sub>w(WE)</sub>      | Write Pulse Time                    | 55  | —   | ns    |
| t <sub>su(A-WEH)</sub>  | Address setup time for WE#          | 10  | —   | ns    |
| t <sub>su(CE-WEH)</sub> | Card Enable setup time for WE#      | 0   | —   | ns    |
| t <sub>su(D-WEH)</sub>  | Data setup time for WE#             | 30  | —   | ns    |
| t <sub>h(D)</sub>       | Data hold time                      | 10  | —   | ns    |
| t <sub>rec(WE)</sub>    | Data record time from WE#           | 15  | —   | —     |
| t <sub>dis(WE)</sub>    | Output disable time from WE#        | —   | 45  | ns    |
| t <sub>en(WE)</sub>     | Output enable time from WE#         | 5   | —   | ns    |
| t <sub>su(OE-WE)</sub>  | Output Enable setup time for WE#    | 10  | —   | ns    |
| t <sub>h(OE-WE)</sub>   | Output Enable hold time from WE#    | 10  | —   | ns    |



**I/O ACCESS READ AND WRITE AC CHARACTERISTIC**

| Symbol             | Parameter                         | Min | Max | Units |
|--------------------|-----------------------------------|-----|-----|-------|
| $t_{d(IORD)}$      | Data Delay after IORD#            | —   | 45  | ns    |
| $t_{h(IORD)}$      | Data Hold following IORD#         | 5   | —   | ns    |
| $t_{w(IORD)}$      | IORD# pulse width                 | 55  | —   | ns    |
| $t_{suA(IORD)}$    | Address setup time for IORD#      | 15  | —   | ns    |
| $t_{hA(IORD)}$     | Address hold time for IORD#       | 10  | —   | ns    |
| $t_{suCE(IORD)}$   | Card Enable setup time for IORD#  | 5   | —   | ns    |
| $t_{hCE(IORD)}$    | Card Enable hold time from IORD#  | 10  | —   | ns    |
| $t_{suREG(IORD)}$  | REG setup time for IORD#          | 5   | —   | ns    |
| $t_{hREG(IORD)}$   | REG Hold time from IORD#          | 0   | —   | ns    |
| $t_{dINP(IORD)}$   | INPACK delay falling from IORD#   | 0   | 45  | ns    |
| $t_{dRNP(IORD)}$   | INPACK delay rising from IORD#    | —   | 45  | ns    |
| $t_{dIO16(IORD)}$  | IOIS16 delay falling from address | —   | 35  | ns    |
| $t_{dRIO16(IORD)}$ | IOIS16 delay rising from address  | —   | 35  | ns    |
| $t_{su(IOWR)}$     | Data setup time for IOWR#         | 15  | —   | ns    |
| $t_{h(IOWR)}$      | Data hold time from IOWR#         | 5   | —   | ns    |
| $t_{w(IOWR)}$      | IOWR# pulse width                 | 55  | —   | ns    |
| $t_{suA(IOWR)}$    | Address setup time for IOWR#      | 15  | —   | ns    |
| $t_{hA(IOWR)}$     | Address hold time from IOWR#      | 10  | —   | ns    |
| $t_{suCE(IOWR)}$   | Card Enable setup time for IOWR#  | 5   | —   | ns    |
| $t_{hCE(IOWR)}$    | Card Enable hold time from IOWR#  | 10  | —   | ns    |
| $t_{suREG(IOWR)}$  | REG setup time for IOWR#          | 5   | —   | ns    |
| $t_{hREG(IOWR)}$   | REG hold tme from IOWR#           | 0   | —   | ns    |



**TRUE-IDE PIO MODE READ AND WRITE CHARACTERISTICS**

| Symbol          | Parameter                          | Min | Max | Units |
|-----------------|------------------------------------|-----|-----|-------|
| t <sub>0</sub>  | Cycle time                         | 80  | —   | ns    |
| t <sub>1</sub>  | Address setup time for IORD#/IOWR# | 10  | —   | ns    |
| t <sub>9</sub>  | Address hold time from IORD#/IOWR# | 10  | —   | ns    |
| t <sub>2</sub>  | IORD#/IOWR# pulse width            | 55  | —   | ns    |
| t <sub>2i</sub> | IORD#/IOWR# recovery time          | 20  | —   | ns    |
| t <sub>5</sub>  | Data setup time for IORD#          | 10  | —   | ns    |
| t <sub>6</sub>  | Data setup time for IOWR#          | 5   | —   | ns    |
| t <sub>6Z</sub> | Output disable time from IORD#     | —   | 20  | ns    |
| t <sub>3</sub>  | Data setup time for IOWR#          | 15  | —   | ns    |
| t <sub>4</sub>  | Data hold following IOWR#          | 5   | —   | ns    |

**TRUE-IDE MDMA MODE READ AND WRITE CHARACTERISTICS**

| Symbol                              | Parameter                             | Min | Max | Units |
|-------------------------------------|---------------------------------------|-----|-----|-------|
| t <sub>0</sub>                      | Cycle time                            | 80  | —   | ns    |
| t <sub>0</sub>                      | IORD#/IOWR# pulse width               | 55  | —   | ns    |
| t <sub>E</sub>                      | IORD# data access                     | —   | 45  | ns    |
| t <sub>F</sub>                      | Data hold following IORD#             | 5   | —   | ns    |
| t <sub>G</sub>                      | Data setup time for IORD#/IOWR#       | 10  | —   | ns    |
| t <sub>H</sub>                      | Data hold following IOWR#             | 5   | —   | ns    |
| t <sub>I</sub>                      | DMACK# setup time for IORD#/IOWR#     | 0   | —   | ns    |
| t <sub>J</sub>                      | DMACK# hold following IORD#/IOWR#     | 5   | —   | ns    |
| t <sub>KR</sub> , t <sub>KW</sub>   | IORD#/IOWR# recovery time             | 20  | —   | ns    |
| t <sub>L,R</sub> , t <sub>L,W</sub> | IORD#/IOWR# to DMARQ delay            | —   | 35  | ns    |
| t <sub>M</sub>                      | CS0#, CS1# setup for IORD#/IOWR#      | 5   | —   | ns    |
| t <sub>N</sub>                      | CS0#, CS1# hold following IORD#/IOWR# | 10  | —   | ns    |
| t <sub>Z</sub>                      | Output disable time from DMACK#       | —   | 25  | ns    |

**TRUE-IDE IDMA MODE READ AND WRITE CHARACTERISTICS**

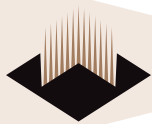
The interface timing in the True-IDE UDMA modes is not only depending on the interface hardware, but also on the correct setup of the UDMA registers in the firmware, according to the UDMA transfer mode selected by the host. With a correct register setup, the interface timing complies to the UDMA Mode 0 to Mode 4 timing specifications of the CF Specification Revision 4.1, and to the UDMA Mode 0 to Mode 4 timing specifications of the ATA/ATAPI-6 Standard.



### PIN ASSIGNMENTS & PIN TYPE

| TBD        |                         |            |
|------------|-------------------------|------------|
| Pin Number | Signal Name             | Pin Type   |
| A02-A15    | NC                      | No Connect |
| B01-B15    | NC                      | No Connect |
| C01-C15    | NC                      | No Connect |
| D01-D03    | NC                      | No Connect |
| D04        | GND                     | Ground     |
| D05        | GND                     | Ground     |
| D06        | IOCS16# (IOIS16#) (WP)  | O          |
| D07        | IORDY (WAIT#)           | O          |
| D08        | DMACK# (REG#)           | I          |
| D09        | CSEL#                   | I          |
| D10        | PDIAG# (STSCHG#) (BVD1) | I/O        |
| D11        | GND                     | Ground     |
| D12        | GND                     | Ground     |
| D13-D15    | NC                      | No Connect |
| E01-E03    | NC                      | No Connect |
| E04        | GND                     | Ground     |
| E05        | DASP# (SPKR#) (BVD2)    | I/O        |
| E06        | DMARQ (INPACK#)         | O          |
| E07        | WE#                     | I          |
| E08        | CS1# (CE2#)             | I          |
| E09        | CS0# (CE1#)             | I          |
| E10        | IORD#                   | I          |
| E11        | D00                     | I/O        |
| E12        | GND                     | Ground     |
| E13-E15    | NC                      | No Connect |
| F01-F03    | NC                      | No Connect |
| F04        | V <sub>cc</sub>         | Power      |
| F05        | NC                      | No Connect |
| F06        | INTRQ (IREQ#) (READY)   | O          |
| F07        | IOWR#                   | I          |
| F08        | ATASEL# (OE#)           | I          |
| F09        | D08                     | I/O        |
| F10        | D14                     | I/O        |
| F11        | D09                     | I/O        |
| F12        | D10                     | I/O        |
| F13-F15    | NC                      | No Connect |
| G01-G03    | NC                      | No Connect |
| G04        | V <sub>cc</sub>         | Power      |
| G05        | V <sub>cc</sub>         | Power      |
| G06        | NC                      | No Connect |
| G07        | GND                     | Ground     |
| G08        | GND                     | Ground     |
| G09        | GND                     | Ground     |
| G10        | GND                     | Ground     |
| G11        | D01                     | I/O        |
| G12        | D15                     | I/O        |
| G13-G15    | NC                      | No Connect |
| H01-H03    | NC                      | No Connect |
| H04        | V <sub>cc</sub>         | Power      |
| H05        | NC                      | No Connect |
| H06        | NC                      | No Connect |
| H07        | GND                     | Ground     |

| TBD        |                 |            |
|------------|-----------------|------------|
| Pin Number | Signal Name     | Pin Type   |
| H08        | GND             | Ground     |
| H09        | GND             | Ground     |
| H10        | D07             | I/O        |
| H11        | D04             | I/O        |
| H12        | V <sub>cc</sub> | Power      |
| H13-H15    | NC              | No Connect |
| J01-J03    | NC              | No Connect |
| J04        | RESET# (RESET)  | I          |
| J05        | NC              | No Connect |
| J06        | GND             | Ground     |
| J07        | GND             | Ground     |
| J08        | GND             | Ground     |
| J09        | V <sub>cc</sub> | Power      |
| J10        | D12             | I/O        |
| J11        | V <sub>cc</sub> | Power      |
| J12        | V <sub>cc</sub> | Power      |
| J13-J15    | NC              | No Connect |
| K01-K03    | NC              | No Connect |
| K04        | NC              | No Connect |
| K05        | A03             | I          |
| K06        | A02             | I          |
| K07        | A05             | I          |
| K08        | A10             | I          |
| K09        | D05             | I/O        |
| K10        | D03             | I/O        |
| K11        | D11             | I/O        |
| K12        | V <sub>cc</sub> | Power      |
| K13-K15    | NC              | No Connect |
| L01-L03    | NC              | No Connect |
| L04        | GND             | Ground     |
| L05        | A00             | I          |
| L06        | A01             | I          |
| L07        | A06             | I          |
| L08        | A09             | I          |
| L09        | D06             | I/O        |
| L10        | D13             | I/O        |
| L11        | EXTTRIG         | I/O        |
| L12        | GND             | Ground     |
| L13-L15    | NC              | No Connect |
| M01-M03    | NC              | No Connect |
| M04        | GND             | Ground     |
| M05        | GND             | Ground     |
| M06        | A04             | I          |
| M07        | A07             | I          |
| M08        | A08             | I          |
| M09        | EXTPWR          | Power      |
| M10        | D02             | I/O        |
| M11        | GND             | Ground     |
| M12        | GND             | Ground     |
| M13-M15    | NC              | No Connect |
| N01-N15    | NC              | No Connect |
| P01-P15    | NC              | No Connect |
| R01-R15    | NC              | No Connect |



### SIGNAL DESCRIPTION

| Signal Name             | Dir.  | Description   |
|-------------------------|-------|---|
| CS0# (CE1#)             | I,U   | Card Enable 1   |
| CS1# (CE2#)             |       | Card Enable 2   |
| DMACK# (REG#)           | I     | DMA Acknowledge (Attribute Memory or I/O Enable)  |
| WE#                     | I,U   | Memory Write Enable   |
| ATASEL# (OE#)           |       | True-IDE Mode select (Output Enable)  |
| IOWR# (STOP)            |       | I/O Write Enable (Terminate ultra DMA data burst)   |
| IOR#                    |       | I/O Read Enable   |
| CSEL#                   |       | True-IDE Master/Slave select  |
| RESET# (RESET)          |       | Reset signal. This pin includes an input filter that filters pulses shorter than about 40 ns. |
| A10..A00                | I/O   | Address Bus. Unused pins may be left open, or connected to GND.                               |
| D15..D00                |       | Data Bus  |
| DMARQ (INPACK#)         | O,U   | DMA Acknowledge (Input Acknowledge)   |
| INTRQ (IREQ#) (READY)   |       | Interrupt Request (Interrupt Request) (Ready/Busy signal )                                    |
| PDIAG# (STSCHG#) (BVDI) |       | True-IDE DIAG (Status Change ) (Unsupported)  |
| DASP# (SPKR#)(BVD2)     | I/O,U | True-IDE DASP (Unsupported) (Unsupported)   |
| IORDY (WAIT#)           |       | I/O Ready (UDMA DDMARDY#, DSTROBE) (Wait)   |
| IOCS16# (IOIS16#) (WP)  | O     | Word Data Transfer (I/O is 16 bit signal ) (Write Protect)                                    |
| EXTTRIG                 | I, U  | External Secure Erase Trigger Input   |
| EXTPWR                  | PWR   | External Backup Power Input   |

### TYPICAL SERIES TERMINATION FOR ULTRA DMA

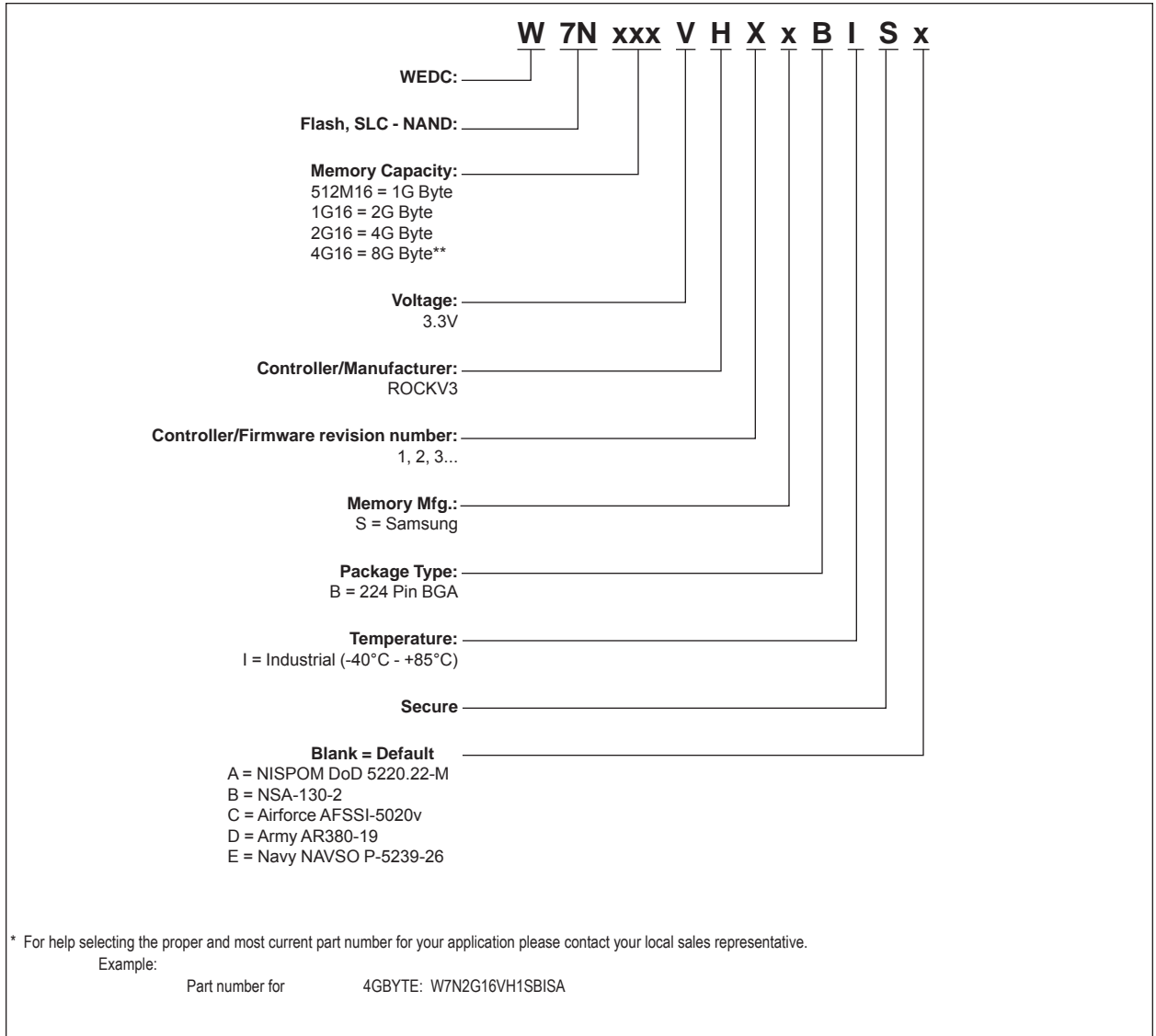
| Signal                    | Host Termination | Device Termination |
|---------------------------|------------------|--------------------|
| IOR# (HDMARDY#, HSTROBE)  | 22 ohm           | 82 ohm             |
| IOWR# (STOP)              | 22 ohm           | 82 ohm             |
| CS0#, CS1#                | 33 ohm           | 82 ohm             |
| A00, A01, A02             | 33 ohm           | 82 ohm             |
| DMACK#                    | 22 ohm           | 82 ohm             |
| D00 through D15           | 33 ohm           | 33 ohm             |
| DMARQ                     | 82 ohm           | 22 ohm             |
| INTRQ                     | 82 ohm           | 22 ohm             |
| IORDY (DDMARDY#, DSTROBE) | 82 ohm           | 22 ohm             |
| RESET#                    | 33 ohm           | 82 ohm             |

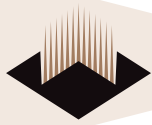
Note: Host Interface Terminator Resistors are at the discretion of the user, but are required for all Ultra DMA modes according to the ATA/ATAPI-6 Specification and the CFA CompactFlash Specification 4.1. Only those signals needing termination are listed in this table. If a signal is not listed, series termination is not needed for operation in an Ultra DMA mode. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable or board trace impedance.





Part Numbering Guide





## Document Title

Secure Embedded SLC NAND SSD PBGA

## Revision History

| Rev # | History  | Release Date | Status   |
|-------|--|--------------|----------|
| Rev 0 | Initial Release  | October 2009 | Advanced |
| Rev 1 | Changes (2, 3, 11)<br>1.1 Correct spelling of "pin."<br>1.2 Correct spelling of "serial" and "encoding."<br>1.3 Change dimensions to "MAX" for "width and height." |              |          |