System in a Package

Microsemi®

System in a Package (SiP)

SiP is a functional system or sub-system assembled into a single package. Typically it will contain two or more dissimilar die. For example:

- The combination of a processor, gate array, ASIC, RAM and flash memories.
- These can be combined with other components such as sensors, triggers, passives, MEMS, voltage regulators, etc.

These are then assembled on an interposer or substrate to create a customized, integrated product for a specific application. Within the SiP, the designer can utilize bare die (wire bond or flip chip), FBGA/CSP packaged devices, stacked die or stacked packages.

The benefits of this technology are:

- Greater functionality in a time-to-market window that cannot be met through silicon integration; increased density and performance.
- Reduced board area, weight and routing complexity at the PCB level. Board layer reduction and performance enhancements reduces PCB costs.
- Design optimization through use of the most cost-effective silicon solutions and assembling different semiconductor technologies, die geometries, or chips from different fabs in the same package.
- Value added of high-speed designs, assembly processes and material set incorporated into the SiP.
- Allows the OEM to upgrade products by using die-shrinks in the same package.

Microsemi's Approach to SiP

Microsemi provides a one-stop, DMEA trusted, on-shore source for concept analysis, design, assembly, anti-tamper and test of high reliability defense-aerospace System in a Package (SiP) semiconductors. The value you will receive as a customer of Microsemi includes:

- Ability to combine COB and SMT to optimize density, control costs and maximize flexibility of design.
- Program and vendor management of all elements of the product.
- Obsolesence management.
- Die revision control.
- Package and material selection for optimization of electrical and environmental performance, thermal management, PCB second level reliability and cost.
- Plastic encapsulation or hermetic sealing; laminate or ceramic based packages. QFP, BGA or customer specified packages.
- Complete turnkey assembly; wire bond, flip chip attach, and specialized die processing including redistribution, wafer dicing and die stacking techniques.
- Qualification can be performed by Microsemi including preconditioning, bias life test, temp cycle, 85°C/85RH moisture test.

- **Facility:** Microsemi's high reliability products are manufactured and tested in accordance with MIL-PRF-38534 (Class H and K) and MIL-PRF-38535 (Class Q) Certified.
  - — Within this facility Microsemi also maintains a DoD secure area for design, manufacture and testing of classified products.
  - — Microsemi standard and custom hermetic products are available as Class K

Program Review and Documentation

Microsemi's engineering team will work closely with the customers engineering team to define and specify all aspects of the product, including:

- Co-develop statement of work (SOW).
- Conversion of component schematic to die schematic; netlist reference design; netlist/schematic documentation and review.
- Environmental requirements.
- Qualification requirements.
- Electrical test and characterization definitions.
- Package definition.
- Power requirements vs. proposed package design.
- Creation of the initial layout specification.
- Initial die placement and floor planning/routing study & pre and post layout simulation.
- Pre and post thermal and mechanical evaluation.
- Initial Design Review, prior to layout; PDR and CDR.

Design for Electrical Performance

- Analog and digital Design
- FPGA (Actel, Altera, Xilinx) design and simulation
- Firmware design (C, Assembly, Script)
- Controlled impedance, differential pairs, low inductance designs with experience in high speed design techniques.
- Pre and post layout electrical simulation for crosstalk, timing and signal integrity.
- Spice (HSpice), ELDO, EBD and IBIS modeling.
- Schematic in DX Designer or ORCAD format.
- Software tools include — Mentor Graphics PADS, HyperLynx, Solidworks, PROe; AutoCAD; PakSi, CF Design, Sigrity signal and power integrity software.

Thermal Management and Cooling of Complex Packages

Microsemi engineers use the following techniques to insure your SiP performs over the thermal environment required:

- Pre and post layout thermal modeling to drive die position, material selection and ball arrangement.
- Thermal vias and balls, embedded heat sinks, added copper layers, enhanced seal ring and lid placement.
- Optimized package design, component placement and material selection.
- Electrical component characterization over target temperature extremes to establish power requirements.
- Die and component selection with low power performance and low power operating features.

Environmental and Electrical Testing:

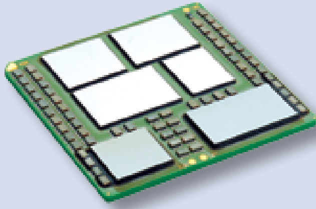
- Hardware and software test engineering services.
- Military, industrial or custom defined temperature ranges.
- Electrical testing based on leading edge Agilent, Teradyne and Megatest equipment.
- Cold/hot chambers for extended environment testing of processor, logic, DRAM, SRAM, and Flash.
- Full dynamic or static burn-in.
- Full custom test development.

Information Assurance

Microsemi has secure anti-tamper technology for the protection of sensitive die, reducing access to data and reverse engineering of the chip. This technology can protect company intellectual property, help meet DoD critical technology requirements and enable FMS.

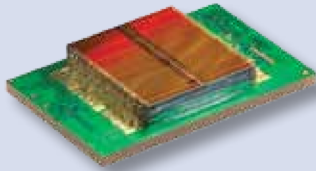
- Multiple techniques designed specifically for chip level anti-tamper.
- Full ITAR protocols and training established.
- Combining sensors, triggers and encryption to SiP products.
- DMEA accreditation of trust.

Examples of WEDC's SiP Capability



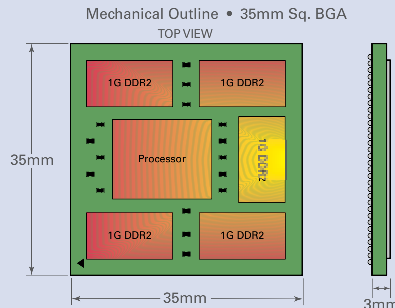
- Custom 18 layer, 40mm BGA.
- Over 50,000 vias and 75micron traces/spaces.
- High yield flip chip assembly of wide aspect ratio die.
- Internally developed test program with more than five million lines of code. Experience with test and test development for large gate array and ASIC custom designs.
- Incredible density enhancements over monolithic approach.
- Controlled impedance, low inductance via design.
- Density: reduced PCB layer count.
- Reliability, reduced part count, reduced mother board I/O.
- HighTCE interposer provides match with PCB.

WEDC offers a family of standard COTS SDRAM, DDR, DDR2, DDR3, flash and SRAM in PBGA and QFP packages. Benefits include:

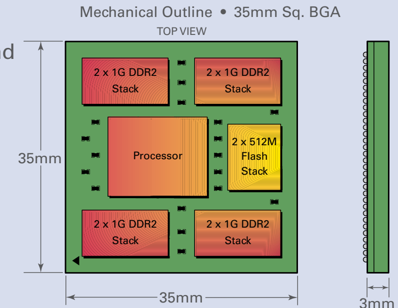


- Multiple program wins leading to volume production for use in density challenged applications.
- Volume die utilization which leverages COTS standard silicon.
- Upgrade path to higher density memory.
- Density enhancement of 25% to 60% over monolithic approach.
- Reduced part count and component I/O for better utilization of PCB routing.
- Provides wide organizations in a standard component.
- SDRAM, DDR, DDR2, DDR3 densities to 1GByte in standard PBGA component.
- Flash densities to 256 MByte in standard PBGA component.
- Third party 2nd level reliability data.

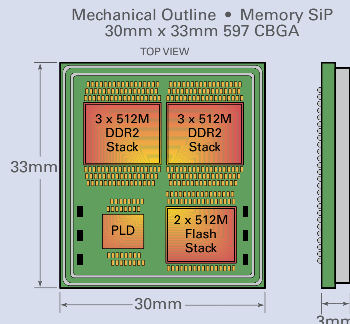
A processor plus memory SiP. Typical memory may be 256MByte to 2GByte of DRAM. This approach allows upgrading memory as higher density become required.

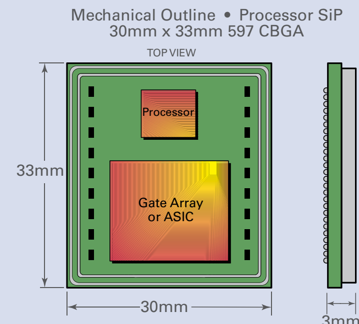


A similar design can incorporate DRAM and flash in the same SiP.



These two devices can be used separately or in tandem to form a complete system or the devices in these packages can be combined into a single dual-cavity package for even higher density and reduced board I/O.





Microsemi Corporation provides leading edge, highly integrated silicon and advanced packaging services that fit the immediate needs of today's engineers. We have extensive experience in advanced semiconductor packaging, high-density memory chip products and state-of-the-art microelectronic multi-chip modules. Our MCPs consist of multiple silicon die on a microcircuit laminate within the confines of a defined molded package providing the density and organization required to meet design needs. We offer a variety of memory configurations utilizing ceramic, hermetic packages and plastic encapsulated microcircuits.

PMG - Microelectronics (also DBA as White Electronic Designs Corp) is a wholly owned subsidiary of Microsemi Corporation

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