



APPLICATION NOTE

DESIGNING HIGH PERFORMANCE SYSTEMS USING WEDC'S REGISTERED SDRAM MCPS

Design of high-performance systems capable of meeting the needs of today's products requires large amounts of SDRAM. To meet the demands of stable functionality over the broad spectrum of operating environments, meet system timing needs, and to support data integrity, the loads presented by the large amount of SDRAMs require the use of registers (drivers) in the address and control signal paths.

Registering is similar to buffering, except that in registering, the data is clocked in and out of the register by the system clock. Therefore registered signals are one clock cycle slower than non-registered signals. Normally extra clock cycles are something to be avoided for high-performance system design, however, in this case the addition of the clock cycle to the SDRAM operation is not as great a factor compared to the overall system performance to be gained by the reduction of the capacitive loading from adding the registers.

WEDC's products such as the 64MB 8Mx72 SDRAM BGA presents the capacitive load of 5 SDRAMs on the address and control signal paths to the memory controller. This load potentially could need to be registered with a driver IC, based on the application. The typical system block diagram showing our 8Mx72 SDRAM connected in a system to a PCI Bridge/Memory controller such as the MPC107 is shown in Figure 1. The SDRAM has a capacitive load of 30pF per MCP, with the potential of multiple SDRAM MCPs being connected to the memory controller.

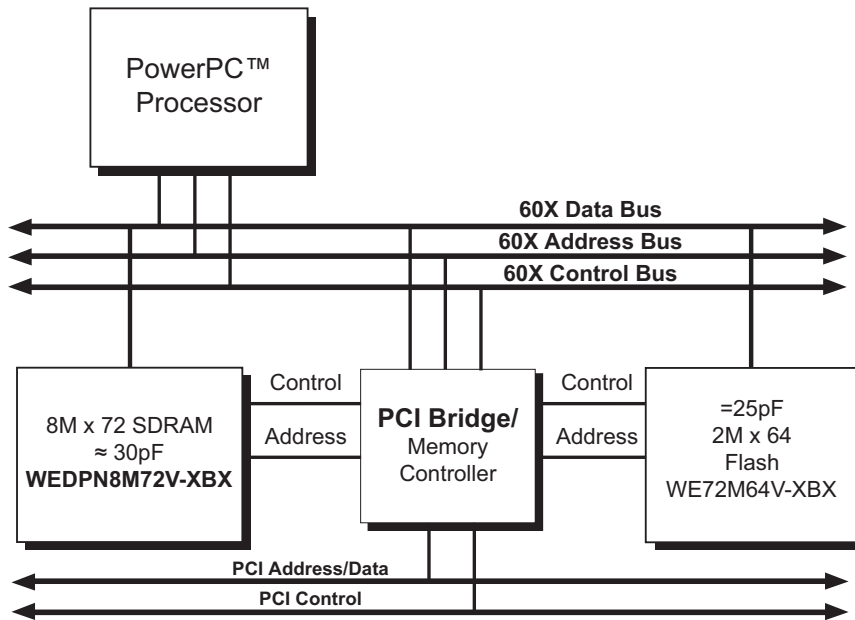


FIGURE 1



Along with the capacitive load from the SDRAM, the memory controller also may need to drive a Flash memory block, such as our 2Mx64 Flash MCP (WE72M64V-XBX), which has a capacitive load of about 25pF, as well as other devices depending on the particular application.

This capacitive loading on the memory controller can cause a dramatic decrease in overall system performance as well as potential data integrity problems due to timing delays in the writing and reading processes. The memory controller is forced to drive more loads than it was designed for, here lies the design potential of WEDC's registered SDRAM MCPs. Refer to Figure 2:

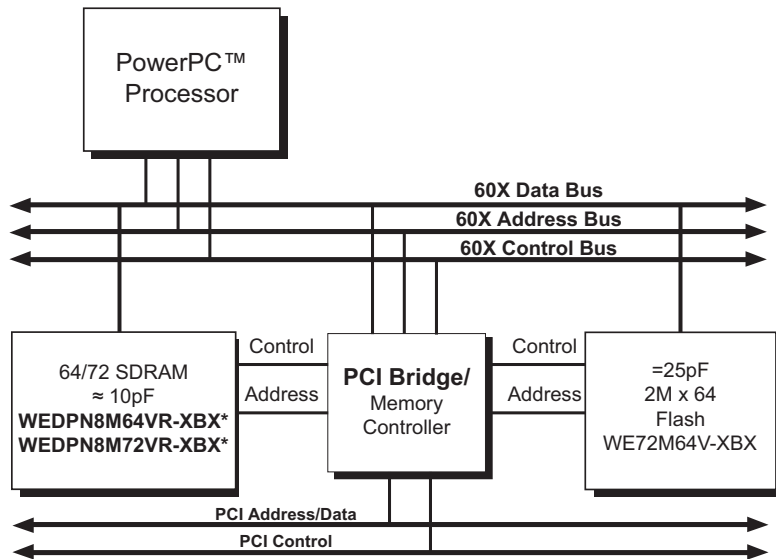


FIGURE 1

Using the same system block diagram from Figure 1, inserting in our registered SDRAM MCP allows the memory controller to see only 10pF of address capacitance instead of 30pF. This allows the memory controller to drive the memory blocks effectively and provide the system performance necessary for high speed applications.

The additional benefits of WEDC's registered SDRAMs are the space savings in the range of 19-59% for board space and 17-40% I/O reduction by bringing the registers off of the system board and into the SDRAM MCP. This also has the benefit of reduced part count on the board, which in turn reduces board routing density and layers and thus overall system board cost.

WEDC REGISTERED SDRAM/DDR PRODUCTS

WEDPN8M64VR-XBX	8M x 64 SDRAM
WEDPN8M72VR-XBX	8M x 72 SDRAM
WEDPN16M64VR-XBX	16M x 64 SDRAM
WEDPN16M72VR-XBX	16M x 72 SDRAM
W3E16M72SR-XBX	16M x 72 DDR SDRAM