

Application Note

The advantages of a PLL based design

Why use an un-buffered DDR SODIMM with a PLL?

As DRAM speeds continue to increase, simplifying the variables at the system to memory interface becomes critical. In the case of the un-buffered DDR SODIMM, our PLL based solution manages all internal clock distribution. This allows us to tune the internal clocks and assure that each part receives a clean clock signal at the proper time. We believe the added benefits the PLL feature adds is worth the extra cost it adds to the DIMM.

Less chance of clock timing errors

Because the module operates on only one clock, we eliminate any possible timing errors that could be introduced by using multiple clocks. When multiple clocks are used in a system, it is possible for the different clocks to get out of phase from each other for various reasons.

Clock loading consistency

To the system looking into the DIMM, each module density and all various configurations available looks the same from a clock perspective (single capacitive load).

Pin-out compatibility

In general this is not an issue, the JEDEC standard specifies 3 separate pairs of differential clocks [CK0 and CK0*, CK1 and CK1*, CK2 and CK2*]. Various configurations use combinations of these three pairs but all use the CK0 and the CK0* as a minimum. Our Modules use the CK0 and CK0* pair so compatibility is not a concern.

Clock management

In PLL based architecture, the system clock only sees the PLL as a load and hence any clock loading behind the PLL is invisible to the system clock. This means the system clock's loading remains constant even when the memory densities and configurations of the module's architecture changes. Contrary to this, the loading will change on the clocks for the un-buffered non-PLL based architecture. On both architectures the loading also changes on the addresses, controls, and data buses with changing memory densities and configurations. By controlling the clock loading using a PLL, we eliminates that variable from the list of changing and shifting signals and this decreases the chances of incompatibility or timing problems.

More control

By using a PLL based design we assure proper frequency and phase matching at each Dram on the module regardless of the modules configuration and or density. In order to achieve the same timing robustness without the PLL it forces this control back to the system level which requires different clock timing for the different module densities and configurations that are populated in the system(usually this is difficult and often overlooked).

System design Simplification

Because the PLL based modules only need one set of differential source clocks it allows the system designer to simplify the number of clock resources routed on the system board. When system designers are looking for a robust solution, simplification is always a step in the right direction.

What about cost

Typically the cost is minimal and is only a small fraction of the modules cost. It is our opinion that the value the PLL brings is well offsets the small cost adder.