FLASH MEMORY OPERATION 1M5

FOR THE FOLLOWING PARTS:

WMF128K8-XXX5 • WF128K16-XCX5 • WF256K16-XCX5 • WF128K32-XXX5 • WF128K64-XG4WX5 • WSF128K16-XXX • WSF128K32-22H2X

PRINCIPLES OF OPERATION

Programming of the device is accomplished by executing the program command sequence. The program algorithm, which is an internal algorithm, automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.3 seconds. Erase is accomplished by executing the erase command sequence. The erase algorithm, which is internal, automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The entire memory is typically erased and verified in three seconds (including pre-programming).

BUS OPERATIONS

Read

The device has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Select ($\overline{CS}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high impedance state.

Standby Mode

The device has two standby modes, a CMOS standby mode ($\overline{CS}$ input held at $V_{CC} \pm 0.5V$). In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.significant guardband (margin to guard against process differences, test skew, etc.). Device power should be calculated to reflect the actual junction temperature, supply voltage, operating frequency, and output loading conditions.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the commands, along with address and data information needed to execute the command. The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Select is low and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of the Write-Enable while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used. Refer to AC Write/Erase/Program characteristics.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Table 3 defines these register command sequences.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

TABLE 1 - BUS OPERATIONS

Operation	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A9	I/O
Read	L	L	X	A_0	A_1	A_9	D_{OUT}
Standby	H	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	HIGH Z
Write	L	H	L	A_0	A_1	A_9	D_{IN}
Verify Sector Protect	L	L	H	L	H	V_{ID}	Code

TABLE 2 - SECTOR ADDRESSES TABLE

	A16	A15	A14	Addr Range
SA_0	0	0	0	00000h-03FFFh
SA_1	0	0	1	04000h-07FFFh
SA_2	0	1	0	08000h-0BFFFh
SA_3	0	1	1	0C000h-0FFFFh
SA_4	1	0	0	10000h-13FFFh
SA_5	1	0	1	14000h-17FFFh
SA_6	1	1	0	18000h-1BFFFh
SA_7	1	1	1	1C000h-1FFFFh

TABLE 3 - COMMAND DEFINITIONS

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

NOTES:

1. Address bit A_{15} = X = Don't Care. Write Sequences may be initiated with A_{15} in either state.
2. Address bit A_{16} = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).
3. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A_{16}, A_{15}, A_{14} will uniquely select any sector.
4. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CS}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CS}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CS}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on D_7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular time. Hence, Data Polling must be performed at the memory location which is being programmed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so will hang up the device, or result in an apparent success according to the data polling algorithm. However, a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 2 illustrates the Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the erase algorithm (Figure 3) sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{\text{WE}}$ pulse in the command sequence and terminates when the data in D7 is “1” (see Write Operation Status section) at which time the device returns to read mode.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{\text{WE}}$, while the command (data) is latched on the rising edge of $\overline{\text{WE}}$. A time-out of 80µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command (30H) to addresses in other sectors desired to be concurrently erased.

The time between writes must be less than 80µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80µs from the rising edge of the last $\overline{\text{WE}}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{\text{WE}}$ occurs within the 80µs time-out window, the timer is reset. (Monitor D3 to determine if the sector erase timer window is still open, see section D3 - Sector Erase Timer.) Any command other than Sector Erase during this time period will reset the device to read mode, ignoring the previous command string. Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 80µs time out from the rising edge of the $\overline{\text{WE}}$ pulse for the last sector erase command pulse and terminates when the data on D7 is "1" (see Write Operation Status section) at which time the device returns to read mode. $\overline{\text{Data}}$ Polling must be performed at an address within any of the sectors being erased.

Figure 3 illustrates the Erase Algorithm using typical command strings and bus operations.

D7 – $\overline{\text{Data}}$ Polling

The device features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the algorithms are in progress or completed.

During the programming algorithm, an attempt to read the device will produce complement data of the data last written to D7. Upon completion of the programming algorithm an attempt to read the device will produce the true data last written to D7. $\overline{\text{Data}}$ Polling is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence.

During the erase algorithm, D7 will be “0” until the erase operation is completed. Upon completion data at D7 is “1”. For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is Valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse.

The $\overline{\text{Data}}$ Polling feature is only active during the programming algorithm, erase algorithm, or sector erase time-out.

See Figure 5 for the $\overline{\text{Data}}$ Polling algorithms.

D6 – Toggle Bit

The device also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During a program or erase algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the device will result in D6 toggling between one and zero. Once the program or erase algorithm cycle is completed, D6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector time out.

It should be noted that either $\overline{CS}$ or $\overline{OE}$ toggling will cause D6 to toggle. See Figure 1 for the Toggle Bit timing specifications and diagrams.

D5 – Exceeded Timing Limits

D5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions D5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling is the only operating function of the device under this condition. The $\overline{CS}$ circuit will partially power down the device under these conditions. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1.

If this failure condition occurs during the sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for additional program or erase operations. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute the program or erase command sequence.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused (other sectors are still functional and can be reused). The device must be reset to use other sectors.

The D5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the system never reads valid data on the D7 bit and D6 never stops toggling. Once the device has exceeded timing limits, the D5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used. The device must be reset to continue using the device.

D3 – Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D3 will remain low until the time-out is complete. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

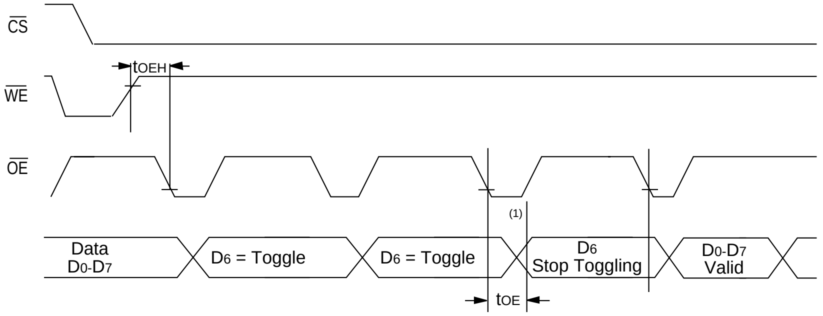
If $\overline{Data}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, D3 may be used to determine if the sector erase timer window is still open. If D3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{Data}$ Polling or Toggle Bit. If D3 is low ("0"), the device will accept additional sector erase commands. To ensure the command has been accepted, the software should check the status of D3 prior to and following each subsequent sector erase command. If D3 were high on the second status check, the command may not have been accepted.

TABLE 4 - WRITE OPERATION STATUS

	Status	D_7	D_6	D_5	D_3	D_2-D_0
In Progress	Byte Program in Program Algorithm	$\overline{D_7}$	Toggle	0	0	Reserved for future use
	Erase Algorithm	0	Toggle	0	1	
Exceeded Time Limits	Byte Program in Program Algorithm	$\overline{D_7}$	Toggle	1	0	Reserved for future use
	Program/Erase in Erase Algorithm	0	Toggle	1	1	

Note: **Performing successive read operations from any address will cause D6 to toggle.**

FIG. 1
AC WAVEFORMS FOR TOGGLE BIT DURING EMBEDDED ALGORITHM OPERATIONS



NOTES:
1. D6 stops toggling (the device has completed the Embedded operation).

DATA PROTECTION

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the read mode. Also, with its control register architecture, alteration of the memory content only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features described below to prevent inadvertent write cycles resulting from Vcc power-up and power-down transitions or system noise.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 3.2V (typically 3.7V). If Vcc < VLKO, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to read mode. Subsequent writes will be ignored until the Vcc level is greater than VLKO. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 3.2V.

Write Pulse Glitch Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CS}$ or $\overline{WE}$ will not initiate a write cycle.

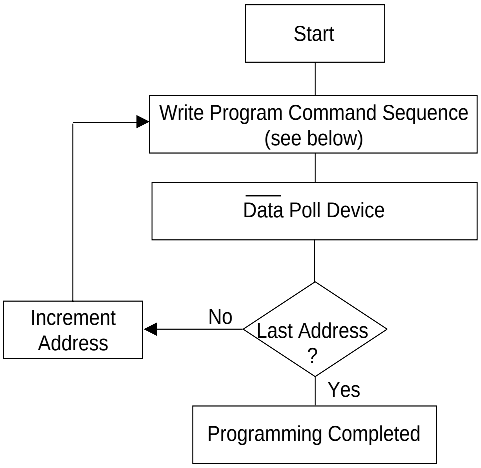
Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CS}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CS}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE}$ = $\overline{CS}$ = VIL and $\overline{OE}$ = VIH will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FIG. 2
PROGRAMMING ALGORITHM



Program Command Sequence (Address/Command):

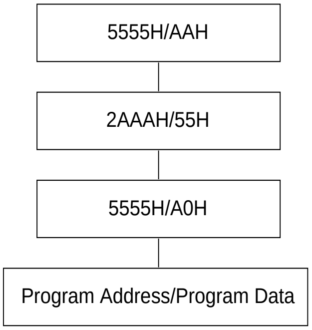


FIG. 3
ERASE ALGORITHM

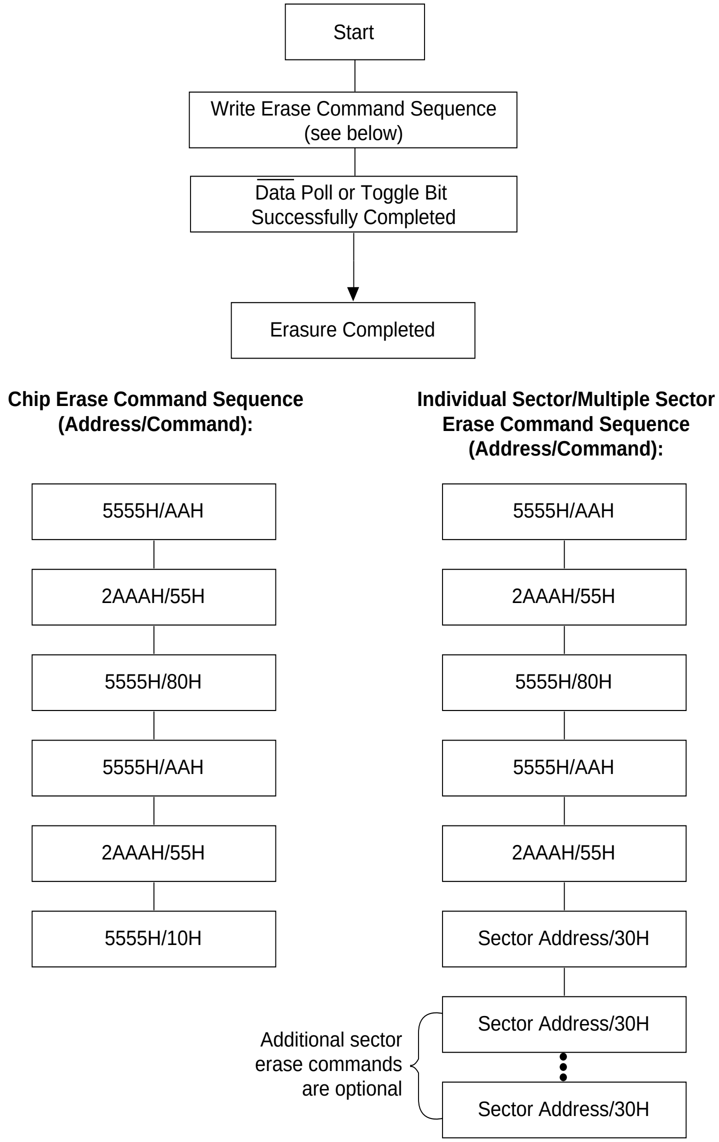
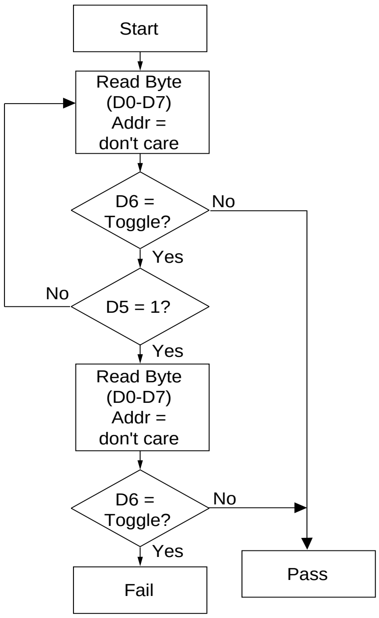
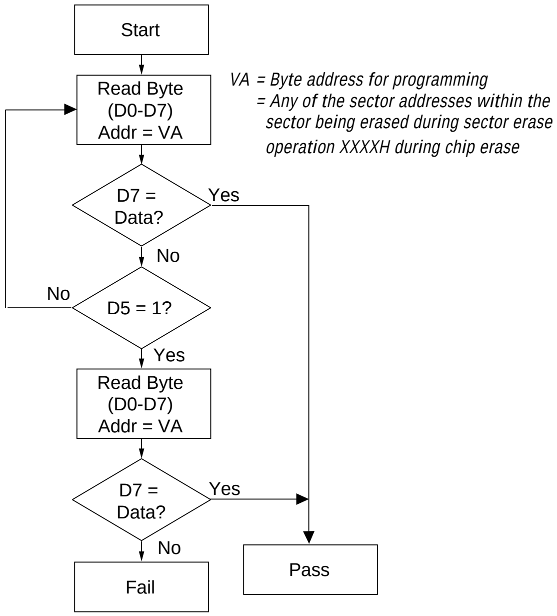


FIG. 4
TOGGLE BIT ALGORITHM



1. D_6 is rechecked even if $D_5 = 1$ because D_6 may stop toggling at the same time as D_5 changes to 1.

FIG. 5
DATA POLLING ALGORITHM



1. D_7 is rechecked even if $D_5 = 1$ because D_6 may change simultaneously with D_5.